Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] An improved FIFO based controller (12) for slave devices attached to the processor bus (14) of a CPU (11) for processing tasks and storing them in a FIFO memory, wherein a task consists of an address (Address) and its associated qualifying bits (ST, ...), comprising:
first logic means (16,17) for enabling valid tasks, i.e. tasks having an address useful for at least one slave device, i.e. that will be followed by corresponding data and inhibiting others (e.g. "address only" tasks) to be presented on a dedicated bus (26); and,
a task management circuit (18) coupled to said first logic means comprising:
a FIFO memory (19) connected to said dedicated bus, provided with a plurality of N storage fields forming a pile, each field being identified by a determined address (Address0, ...) and configured to store any valid task presented on said dedicated bus in parallel to all of said storage fields; and,
second logic means (21) that inhibit the writing of a task in the field (s) of the FIFO memory where a valid task has been entered and enable said writing in the first free field below in the pile.

[c2] The improved FIFO based controller of claim 1 wherein said first logic means comprise:
a task detection circuit (16) coupled to the processor bus that detects valid tasks; and,
a FIFO controller (17) coupled to said task detection circuit that generates an ADD TASK signal to add new tasks to be performed in said FIFO memory, a CLEAR TASK signal that clears all tasks therefrom that have been executed when said corresponding data are available on the processor bus, and a control signal that is applied to gating means (25) for only enabling said valid tasks to be presented on said dedicated bus.

[c3] The improved FIFO based controller of claim 2 wherein a valid bit (V) stored in a register (27-x) is associated to each of said N fields, when it is set to a first binary value, this means that a valid task has been entered in the corresponding field.

[c4] The improved FIFO based controller of claim 3 wherein the output of each pair of consecutive registers (27-0,27-1) is connected to the inputs of a two-way XOR gate (28-0), so that only one output of the N-1 XOR gates is active (at "1") indicating thereby the boundary between the field(s) of the FIFO memory where a valid task has been entered and the remaining free field(s).

[c5] The improved FIFO based controller of claim 1 said second logic means (21) enable said in all the free fields of the FIFO memory instead of only the first free field.

[c6] The improved FIFO based controller of claim 1 further comprising a slave controller (20) coupled to said processor bus and task management circuit.

[c7] The improved FIFO based controller of claim 1 wherein said CPU is a 750 PowerPC microprocessor.